Test Expert Nail Status Legend

#7 "C09201M" Pin:C6.1 Pin:U8.9 — **Net#/Name and list of pins on that net.**

ERROR, no nails found, 1 nail required, invalid Virtual Test Points — **General Error message.**

Nail Priorities:
PRIORITY 4 - 1 Drilled VIA
PRIORITY 4 - 1 SMD VIA on Bottom
PRIORITY 0 - 1 SMD "INTEGRATED CIRCUIT" Pin on Top
PRIORITY 0 - 1 SMD "CAPACITOR" Pin on Top

List of possible PRIORITY Rules that were found or omitted from your Nail Rules. (PRIORITY 0 indicates a rule was omitted.)

2 Nails Available.
2 Virtual Test Points Rejected:
MASK - cannot probe bottom smd VIA at X11.72500, Y6.72500 (Nail conflict with Mask Layer 49)
MASK - cannot probe drilled VIA at X11.72500, Y6.72500 on Bottom (Nail conflict with Mask Layer 49)

List of possible probe points and details as to why they were rejected.)

Error Message	What It Means	What To Do
NO PRIORITY STATEMENTS FIT	None of the Priority Rules you defined in the Nail Rules Dialog provide access to the net in question.	These are usually CAD design problems - typically a via needs to be added to the net. They should be reported (you can print out the Status.asc file) and **someone must determine whether the design can be changed** so these nets become probable- or not. You may also want to review your Nail Rules to determine if a new rule could be added (or an existing rule modified) to allow access to this net.
NAIL MINIMUM	An accessible probe point was found, but a nail/probe was already placed on an adjacent probe point with a higher priority and the new nail / probe will violate NAIL_MIN (nail-to-nail clearance) setting you defined.	If there are just a few of these, you can either add another nail to nail minimum rule and Nail type. Or, you can manually put them in. **However, it may be a design problem that is not fixable.**
NAIL ACCESS	The probe point is too close to an adjacent component body violating the NAIL_ACCESS rule (nail to component body clearance) defined in your nail rules.	Either the desired probe points really are too close to the component bodies (in which case you have a real problem), or the shapes are too big and do not represent the true footprint of the part. In this case, **they need to be corrected in Test Expert, or you need to lower your nail access minimum rule** (or both).
HEIGHT ACCESS	The probe point is conflicting with the height clearance of an adjacent component, violating a HEIGHT_ACCESS rule (nail to component height clearance) defined in your nail rules.	Either the desired probe points really are too close to the component bodies (in which case you have a real problem), or the component heights are too big and do not represent the true height of the part. In this case, **they need to be corrected in Test Expert, or you need to lower your HEIGHT_ACCESS rules** (or both).
MASKING	1. The Mask Layer(s) assigned in your nail rules didn't contain mask data for the object (via or component pin) that you are trying to probe. 2. Mask data exists but is in violation of the mask clearance defined in your Nail Rules.	This is a tricky one. The solder mask data in the CAD may be correct, but the manufacturer may have done something different at the last minute. **It is always best to have a final production-ready board in front of you to verify any solder mask problems.** You may find that there are some large solder mask pads, and some very *small* solder mask pads. By default, Test Expert regards both as legitimate. If you want to use one but not the other, set the MASK CLEARANCE OPTION in the Physical Attributes Nail Rules. *Masking for component pins is only checked if the CHECK_PIN_MASK option is turned on. If your mask layer contains data for the vias, make sure this option is unchecked in the nail rules.